

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In Re Application of:)

Yuval Bachrach)

Examiner: Laforgia C. A.)

Application No: 09/471,637)

Art Unit: 2131)

Filing Date: December 23, 1999)

Confirmation No.: 7753)

For: PHYSICAL LAYER AND DATA)
LINK INTERFACE WITH ADAPTIVE)
SPEED)
_____)Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 41.37(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner of Group 2131, dated November 12, 2003, which finally rejected claims 1-21 in the above-identified application. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

FIRST CLASS CERTIFICATE OF MAILING

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David Castro

(Name of Person Mailing Correspondence)

Signature

May 26, 2005

Date

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF THE CLAIMS

Claims 1-21 are pending in the application and were finally rejected in an Office Action mailed November 12, 2003. Claims 1-21 are the subject of this appeal. A copy of Claims 1-21 as they stand on appeal are set forth in Appendix A.

IV. STATUS OF AMENDMENTS

No amendments have been submitted subsequent to the Final Office Action mailed November 12, 2003.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellant's invention as claimed in claims 1-21 is directed to a network interface device comprising a PHY (Physical Layer) and a MAC (Media Access Control Layer). The PHY and MAC layers communicate with each other. The communication between the PHY and the MAC is in the form of PHY-to-MAC words and MAC-to-PHY words. A PHY-to-MAC word is a word that is sent by the PHY to the MAC, and a MAC-to-PHY word is a word that is sent by the MAC to the PHY. A word may contain data, control information, or both.

Embodiments of the present invention provide a flexible communication interface between the MAC and the PHY so that many data speeds for exchanging information between the PHY and the MAC may be realized in a flexible manner without changing the clock signal frequency. This is accomplished by using information in a word format, where the word format supports a slow-mode PHY-to-MAC word. More specifically, a PHY-to-MAC word has a transmit cycle field. When a PHY-to-MAC word is received by the MAC, the MAC may or may not provide data to the PHY in the "next" MAC-to-PHY word, depending upon whether the transmit cycle field in the PHY-to-MAC word is a 1 or 0.

Loosely stated, the transmit cycle field controls the “flow” of data sent by the MAC to the PHY. If the transmit cycle field in a PHY-to-MAC word is such that the MAC is instructed not to send data in a next MAC-to-PHY word, then this flow of data is effectively decreased. By allowing for the PHY to instruct the MAC when to send data in a next MAC-to-PHY word, many data speeds may be handled in a flexible manner.

Independent claim 1 claims a MAC including at least one PHY-to-MAC port (Specification, page 9, lines 18-22, Fig. 9) to receive signals indicative of PHY-to-MAC words, and at least one MAC-to-PHY port (Specification, page 9, lines 18-22, Fig. 9) to transmit signals indicative of MAC-to-PHY words. The PHY-to-MAC words (Specification, pages 5-7, Figs. 2-6) include slow mode PHY-to-MAC words (Specification, pages 5-6, Fig. 3), where a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word (Specification, page 5, Fig. 3).

Independent claim 8 claims a PHY to transmit and receive signals propagated on a medium, and to communicate with a MAC via PHY-to-MAC words and MAC-to-PHY words, including at least one MAC-to-PHY port (Specification, page 9, lines 18-22, Fig. 9) to receive signals indicative of the MAC-to-PHY words and at least one PHY-to-MAC port (Specification, page 9, lines 18-22, Fig. 9) to transmit signals indicative of the PHY-to-MAC words. The PHY-to-MAC words (Specification, pages 5-7, Figs. 2-6) include slow mode PHY-to-MAC words (Specification, pages 5-6, Fig. 3), where a slow mode PHY-to-MAC word transmitted by the PHY and received by the MAC includes a

transmit cycle field to indicate whether the MAC is requested by the PHY to provide data for transmission on the medium in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word (Specification, page 5, Fig. 3).

Claims 15 claims embodiments of the invention as a system.

VI. GROUNDS OF REJECTIONS TO BE REVIEWED ON APPEAL

A. Whether claims 1, 2, 8, 9, and 15-16 are anticipated under 35 U.S.C. §102(e) by Boucher, et al., US patent 6,427,173 (“Boucher”); whether claims 3, 4, and 6 are patentable under 35 U.S.C. §103(a) over Boucher in view of Rubin, US patent 4,525,795 (“Rubin”); and whether claims 5, 7, 10-14, and 17-21 are patentable under 35 U.S.C. §103(a) over Boucher in view of Findlater, et al., U.S. patent 6,385,208 (“Findlater”).

VII. ARGUMENT

A. Claims 1, 2, 8, 9, and 15-16 are not anticipated under 35 U.S.C. §102(e) by Boucher; claims 3, 4, and 6 are patentable under 35 U.S.C. §103(a) over Boucher in view of Rubin; and claims 5, 7, 10-14, and 17-21 are patentable under 35 U.S.C. §103(a) over Boucher in view of Findlater.

Claims 1-21 stand or fall together. In the final office action mailed 12 November 2003 ("Office Action"), claims 1, 2, 8, 9, 15, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Boucher. Specifically, beginning at the top of page 4 of the Office Action, it is stated that Boucher teaches the claim limitation that the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. In support of this assertion, the Office Action makes reference to Boucher, figures 4B, 4D, 6, 9, and 22, as well as column 8, lines 28-63; column 9, lines 13-66; column 10, lines 18-34; column 11, lines 22-46; and column 17, lines 9-34.

Boucher does not teach this claim limitation. Boucher teaches how the processing of received data packets may be accelerated, where messages selected for "fast-path" processing avoid the standard protocol stack and instead are handled by special purpose hardware. Boucher does not teach that communication between a MAC and a PHY is word based, and more particularly, Boucher does not teach a word based interface between a MAC and a PHY where a slow mode PHY-to-MAC word has a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

Furthermore, Applicant respectfully believes that the argument in the Office Action, item number 6, pages 2-3, incorrectly considers communication of the PHY over the medium as somehow anticipating the present invention. For example, near the top of

page 3 of the Office Action, it is stated that “the MAC is responsible for informing the PHY which speed the data will be received at, i.e. 10Base-T, 10Base-T2, etc.” However, the present invention is directed to how a MAC and a PHY communicate with each other via a word based interface. The present invention is not directly concerned with how a PHY communicates with another PHY over a medium.

By allowing for a flexible word based interface between a PHY and a MAC, it is possible for a MAC to be used with various types of PHYs from perhaps different manufacturers. In some instances, the MAC may be able to transfer data to a PHY faster than the PHY is able to transmit data on the medium. In such a case, a slow mode is used whereby not all words transmitted from the MAC to the PHY contain data to be transmitted over the medium. In this way, various data link speeds may be supported without changing the clock signal frequency between the MAC and the PHY. (See page 5, lines 13-20, and page 6, lines 5-13 of the present application.) This is the motivation for the present invention. This practical feature is realized by inventions defined by the present claims, specifically, the claim limitation reciting a slow mode PHY-to-MAC word, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

In the Office Action, claims 3, 4, and 6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Rubin. However, Rubin is cited merely for teaching words that are each 12 bits wide. Consequently, for the reasons given above regarding Boucher, claims 3, 4, and 6 are believed patentable over Boucher and Rubin.

In the Office Action, claims 5, 7, 10-14, and 17-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Findlater. In the Office Action, page 9, Findlater is cited for merely teaching PHY-to-MAC words that have data fields in various bit positions. But Applicant asserts that nowhere does Findlater teach a word based interface, and more particularly, nowhere does Findlater teach or suggest the claimed limitation of a slow mode PHY-to-MAC word that includes a transmit cycle field to indicate whether the MAC is to provide data in the next MAC-to-PHY word. Consequently, for the reasons given above regarding Boucher, claims 5, 7, 10-14, and 17-21 are believed patentable over Boucher in view of Findlater. Withdrawal of the rejections is respectfully requested.

VIII. CONCLUSION

For the reasons stated above, claims 1-21 are not anticipated under 35 U.S.C. § 102(e) by Boucher and are patentable under 35 U.S.C. § 103(a) over Boucher in view of Rubin and Findlater. Appellant respectfully requests that the Board reverse the rejections of the claims 1-21 under 35 U.S.C. § 102(e) / § 103(a) and direct the Examiner to enter a Notice of Allowance for claims 1-21.

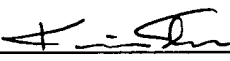
Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Appellant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: May 26, 2005



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Patent

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APPENDIX A FOR APPEAL BRIEF UNDER 37 C.F.R. § 41.37(A)

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1. (Previously Presented) A MAC comprising:

at least one PHY-to-MAC port to receive signals indicative of PHY-to-MAC words; and

at least one MAC-to-PHY port to transmit signals indicative of MAC-to-PHY words;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

2. (Previously Presented) The MAC as set forth in claim 1, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word received by the MAC from the PHY indicates that the MAC is to provide data in the next MAC-to-PHY word.

3. (Original) The MAC as set forth in claim 1, wherein the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

4. (Original) The MAC as set forth in claim 1, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

5. (Original) The MAC as set forth in claim 4, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

6. (Previously Presented) The MAC as set forth in claim 4, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word received by the MAC from the PHY indicates that the MAC is to provide data in the next MAC-to-PHY word; and

the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

7. (Original) The MAC as set forth in claim 6, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

8. (Previously Presented) A PHY to transmit and receive signals propagated on a medium, and to communicate with a MAC via PHY-to-MAC words and MAC-to-PHY words, the PHY comprising:

at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words; and

at least one PHY-to-MAC port to transmit signals indicative of the PHY-to-MAC words; wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word transmitted by the PHY and received by the MAC includes a transmit cycle field to indicate whether the MAC is requested by the PHY to provide data for transmission on the medium in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

9. (Previously Presented) The PHY as set forth in claim 8, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word transmitted by the PHY to the MAC indicates that the MAC is to provide data in the next MAC-to-PHY word.

10. (Original) The PHY as set forth in claim 8, wherein the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

11. (Original) The PHY as set forth in claim 8, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

12. (Original) The PHY as set forth in claim 11, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

13. (Previously Presented) The PHY as set forth in claim 11, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word transmitted by the PHY to the MAC indicates that the MAC is to provide data in the next MAC-to-PHY word; and

the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

14. (Original) The PHY as set forth in claim 13, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

15. (Previously Presented) A computer system comprising:

a MAC; and

a PHY to receive and transmit signals propagated on a medium and connected to the MAC so that the MAC provides MAC-to-PHY words to the PHY and the PHY provides PHY-to-MAC words to the MAC;

wherein the PHY-to-MAC words and the MAC-to-PHY words are synchronously paired so that the MAC provides one MAC-to-PHY word to the PHY while the PHY provides one PHY-to-MAC word to the MAC;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words having a transmit cycle field;

wherein if the transmit cycle field of a first slow mode PHY-to-MAC word is set to a first value, the first slow mode PHY-to-MAC word being synchronously paired with a first MAC-to-PHY word, then the MAC is requested by the PHY to provide transmit data in a second MAC-to-PHY word for transmission over the medium, where the second MAC-to-PHY word succeeds the first MAC-to-PHY word, and if the transmit cycle field of the first slow mode PHY-to-MAC word is set to a second value different from the first value, then the MAC is requested by the PHY not to include transmit data in the second MAC-to-PHY word.

16. (Original) The computer system as set forth in claim 15, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words.

17. (Original) The computer system as set forth in claim 15, wherein the PHY-to-MAC words and MAC-to-PHY words are 12 bits wide.

18. (Original) The computer system as set forth in claim 15, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

19. (Original) The computer system as set forth in claim 18, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

20. (Original) The computer system as set forth in claim 18, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words; and
the PHY-to-MAC words and MAC-to-PHY words are 12 bits wide.

21. (Original) The computer system as set forth in claim 20, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit

position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.